PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Stefan Marco Koch et al.
Application No.	:	10/521,881
Filed	:	September 28, 2005
For	:	INTER-PROCESSOR COMMUNICATION SYSTEM FOR COMMUNICATION BETWEEN PROCESSORS
Examiner	:	George Giroux
Art Unit	:	2183
Docket No.	:	853663.412USPC
Date	:	November 16, 2009

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL APPELLANTS' BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on March 26, 2009 and in response to the Notification of Non-Compliant Appeal Brief issued by the Examiner and mailed on September 15, 2009. Any required request for extension of time for filing this brief and fees therefor, are dealt with in the accompanying transmittal letter.

This brief amends Section I to identify ST-Ericsson SA as the real party in interest. See 37 CFR 41.8. This brief amends Sections V and VII in response to the Notification of Non-Compliant Appeal Brief. The Examiner indicated the summary in Section V contained "a number of pages of summary and figures which are not directly related to a concise summary of the claims." This brief moves the portions of Section V to which it is believed the Examiner objected to Section VII. The Examiner also indicated references to figures were made in Section V "without any accompanying reference figure numbers." Reference figure numbers have been added to Section V.

I. REAL PARTY IN INTEREST

The real party in interest is ST-Ericsson SA, which has an address at 39 Chemin du Champ des Filles, 1228 Plan-Les-Outes, Geneva, CH.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the real party in interest are unaware of any appeal or interference which may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF CLAIMS

Claims 1-7, 9, 10 and 13-19 are pending and stand rejected. Claims 8, 11, 12 and 20-23 are canceled. As discussed in more detail below, amendments to the claims were submitted after the final rejection and entered by the Examiner for purposes of appeal. All pending active claims are attached hereto as Appendix A, and reflect the amendments entered by the Examiner for purposes of appeal.

Claims 13, 14, 16, 18 and 19 stand rejected under 35 USC Section 102(b) as anticipated by U.S. Patent Publication No. 2002/0055979 by Koch. Claims 1-7, 9, 10, 15 and 17 stand rejected under 35 U.S.C. Section 103(a) as obvious over Koch in view of U.S. Patent No. 6,775,717 issued to Tang.

The rejections of claims 1-7, 9, 10 and 13-19 are appealed.

IV. STATUS OF AMENDMENTS

An amendment after the final Office Action was submitted on January 26, 2009. The amendment addressed informalities in claim 1. The Examiner entered the amendment to claim 1 for purposes of appeal in an Advisory Action mailed on February 13, 2009 (the "First Advisory Action"), in which the Examiner disagreed with the arguments made in response to the final Office Action.

In response to the First Advisory Action, an amendment addressing an informality in claim 1, amending claims 13-17 to clarify the issues presented for appeal, and canceling claims 20-23, was submitted on March 26, 2009. In an Advisory Action mailed on April 15, 2009 (the "Second Advisory Action"), the Examiner entered the amendments for purposes of appeal, and disagreed with the arguments submitted in response to the First Advisory Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This application is a conversion of PCT Application No. PCT/IB03/02813 filed July 16, 2003 into a U.S. National Application. The following summary discusses the subject matter of the appealed claims along with parenthetical references to portions of the specification and drawings that provide support for the claims. The references are provided for exemplary purposes and are not intended to restrict the scope of the claims to the particular embodiments corresponding to the references provided. There are no means-plus-function or step-plus-function claims.

For convenience, Figures 2 and 3 and a more detail discussion of embodiments of the invention appears below in the argument section (as noted above, this material was moved in response to the Notification of Non-Compliant Appeal Brief). For conciseness, references to the text of the specification will be set forth in bold in a condensed manner, for example, page 2, lines 10-14 will appear as **p. 2:10-14**. For brevity, all references to an element in the text and figures of the specification are not set forth in this summary.

Turning to the independent claims, claim 1 is directed to a system comprising: a first processor bus (Figs. 1-3, ref. 10; Fig. 4, Ref. 70; Fig. 5, Ref. 90; **p. 7:3-6**); a first processor (Figs. 1, 2, 4 and 5, Ref. P1; **p. 7:3-6**) on a first clock (Figs. 3 and 6, Ref. clock1; **p. 9:20-24**; **p. 10:16-21**) coupled to the first processor bus; a first direct memory access unit (Figs. 2 and 3, Ref. 45; Fig. 4, Ref. 83; Fig. 5, Ref. 101; **p. 7:15-18**) with a first external direct memory access channel (Fig. 3, ref. 47; Fig. 4, Ref. 85; Fig. 5, Ref. 106; **p. 7:15-17**), the first direct memory access unit being coupled to the first processor bus; a first programmable unit (Figs. 2 and 3, Ref. 34; Fig. 4, Ref. 82; Fig. 5, Ref. 92; **p. 7:20-21**) comprising a first processor interface, the first programmable unit coupled via the first external direct memory access channel to the first direct memory access unit, said first programmable unit being programmable by the first processor via the first processor interface; a first shareable unit (Fig. 2, Ref. 13; Fig. 4, Ref. 76; Fig. 5, Ref. 93; **p. 7:3-7**; **p. 8:3-8**) coupled to the first processor bus; a second processor bus (Figs. 1-3, Ref. 20; Fig. 4, Ref. 80; Fig. 5, Ref. 100; **p. 7:7-9**); a second processor (Figs. 1, 2, 4, and 5, Ref. P2; **p.7:7-9**) on a second clock (Figs. 3 and 6, Ref. clock2; **p. 9:20-24**; **p. 10:16-21**) coupled to the second processor bus; a second direct memory access unit (Figs. 2 and 3; Ref. 35; Fig. 4, Ref. 73; Fig. 5, Ref. 93; **p. 7:22-24**) with a second external direct memory access channel (Fig. 3, Ref.

36; Fig. 4, Ref. 75; Fig. 5, Ref. 96; **p. 7:22-24**), the second direct memory access unit being coupled to the second processor bus; a second programmable unit (Figs. 2 and 3, Ref. 44; Fig. 4, Ref. 72; Fig. 5, Ref. 92; **p. 7:26-28**) comprising a second processor interface, the second programmable unit coupled via the second external direct memory access channel to the second direct memory access unit, said second programmable unit being programmable by the second processor via the second processor interface; and a second shareable unit (Fig. 2, Ref. 23; Fig. 4, Ref. 86; Fig. 5, Ref. 103; **p. 7:3-7**; **p. 8:3-8**) being connected to the second processor bus, wherein the first programmable unit and the second programmable unit each comprises: a direct access unit core (Fig. 3, Ref. 52; Fig. 3, Ref. 62; **p. 10:4-15**); a first external direct memory access channel interface on the first clock (Fig. 3, Ref. 61; Fig. 3, Ref. 53; **p. 10:4-15**); and a second external direct memory access channel interface on the second clock (Fig. 3, Ref. 63; Fig. 3, Ref. 51; **p. 10:4-15**), wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit. (See Figures 2-6 and the description on pages 9-12).

Independent claim 13 is directed to a system comprising: a first processor (Figs. 1, 2, 4 and 5, Ref. P1; **p. 7:3-6**) and a first shareable unit (Fig. 2, Ref. 13; Fig. 4, Ref. 76; Fig. 5, Ref. 93; **p. 7:3-7**; **p. 8:3-8**) coupled to a first bus (Figs. 1-3, ref. 10; Fig. 4, Ref. 70; Fig. 5, Ref. 90; **p. 7:3-6**), the first processor and first shareable unit operating on a first processor clock (Figs. 3 and 6, Ref. clock1; **p. 9:20-24**; **p. 10:16-21**); a second processor (Figs. 1, 2, 4, and 5, Ref. P2; **p.7:7-9**) and a second shareable unit (Fig. 2, Ref. 23; Fig. 4, Ref. 86; Fig. 5, Ref. 103; **p. 7:3-7**; **p. 8:3-8**) coupled to a second bus (Figs. 1-3, Ref. 20; Fig. 4, Ref. 80; Fig. 5, Ref. 100; **p. 7:7-9**), the second processor and second shareable unit operating on a second processor clock (Figs. 3 and 6, Ref. clock2; **p. 9:20-24**; **p. 10:16-21**); a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface (Fig. 3, Refs. 50, 51; **p. 10:10-15**) to the second processor, wherein the first bi-directional channel comprises: a first internal channel (Fig. 3, Ref. 49; **p. 10:22-29**) of a

first DMA unit (Figs. 2 and 3, Ref. 45; **p. 7:15-18**) coupled to the first bus, the first DMA unit configured with a first external channel (Fig. 3, Ref. 54; **p. 9:33**; **p. 10:16-21**) to operate on the first processor clock; and a first internal channel (Fig. 3, Ref. 39; **p. 9:29-30**) of a second DMA unit (Fig. 3, Ref. 35; **p. 9:28-30**) coupled to the second bus, the second DMA unit configured with a first external channel (Fig. 3, Ref. 56; **p. 9:28-30**; **p. 10:16-21**) to operate on the second processor clock; and a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface (Fig. 3, Refs. 60, 52; **p. 10:4-9**) to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus, wherein the second bi-directional channel comprises: a second external channel (Fig. 3, Ref. 55; **p. 9:33**; **p. 10:16-21**) of the first DMA unit to operate on the first processor clock; and a second external channel (Fig. 3, Ref. 57; **p. 10:4-9**; **p.10:16-21**) of the second DMA unit to operate on the second processor clock. (See Figure 3 and the description thereof on pages 9-11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 13, 14, 16, 18 and 19 are unpatentable under 35 USC Section 102(b) as anticipated by U.S. Patent Publication No. 2002/0055979 by Koch.

2. Whether claims 1-7, 9, 10, 15 and 17 are unpatentable under 35 USC Section 103(a) as obvious over Koch in view of U.S. Patent No. 6,775,717 issued to Tang.

In view of the amendments entered by the Examiner for purposes of appeal and the Examiner's comments in the Second Advisory Action, Appellants believe the grounds of rejection to be reviewed on appeal include whether claims 1-7, 9, 10 and 13-19 are unpatentable under 35 USC Section 103(a) as obvious over Koch in view of Tang. Appellants appreciate the Examiner's entry of the amendments after final and the Examiner's cooperation in narrowing the issues presented for appeal. To avoid any waiver, Appellants will address both the grounds for rejection asserted in the Final Office Action and the Examiner's indication in the Second Advisory Action that the claims were obvious over Koch in view of Tang.

VII. ARGUMENT

This invention concerns generally the communication between two or more processors. For example, two processors are operably coupled via a communication channel for exchanging information. A first processor (P1) has a processor bus, a sharable unit, and a DMA unit with two external DMA channels. The DMA unit and the sharable unit are connected to the processor bus. The other processor (P2) also has a processor bus, a sharable unit, and a DMA unit with two external DMA channels. Programmable units are employed enabling the processor to set up the desired communication links. Two bi-directional communication channels are established between the two bus regimes. The arrangement is highly symmetrical and minimizes the number of otherwise needed bus masters for each processor. See page 3 of the application. For convenience, Figures 2 and 3 of the application are produced below.

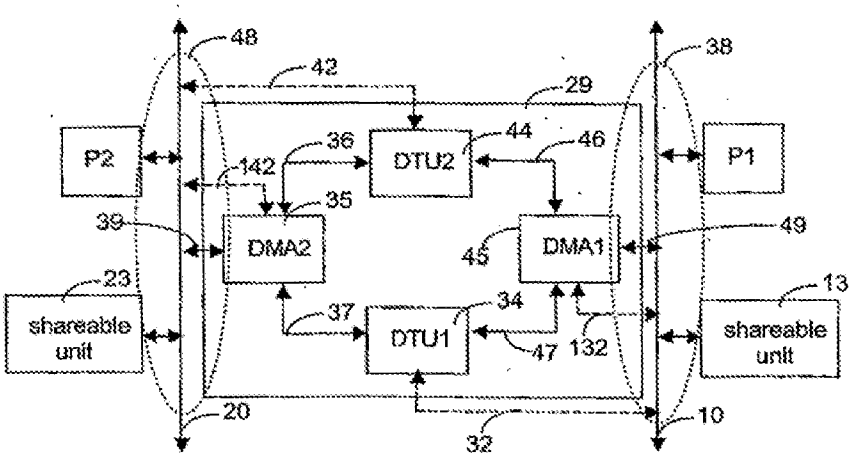

Fig. 2

Figure 2 of the Present Application

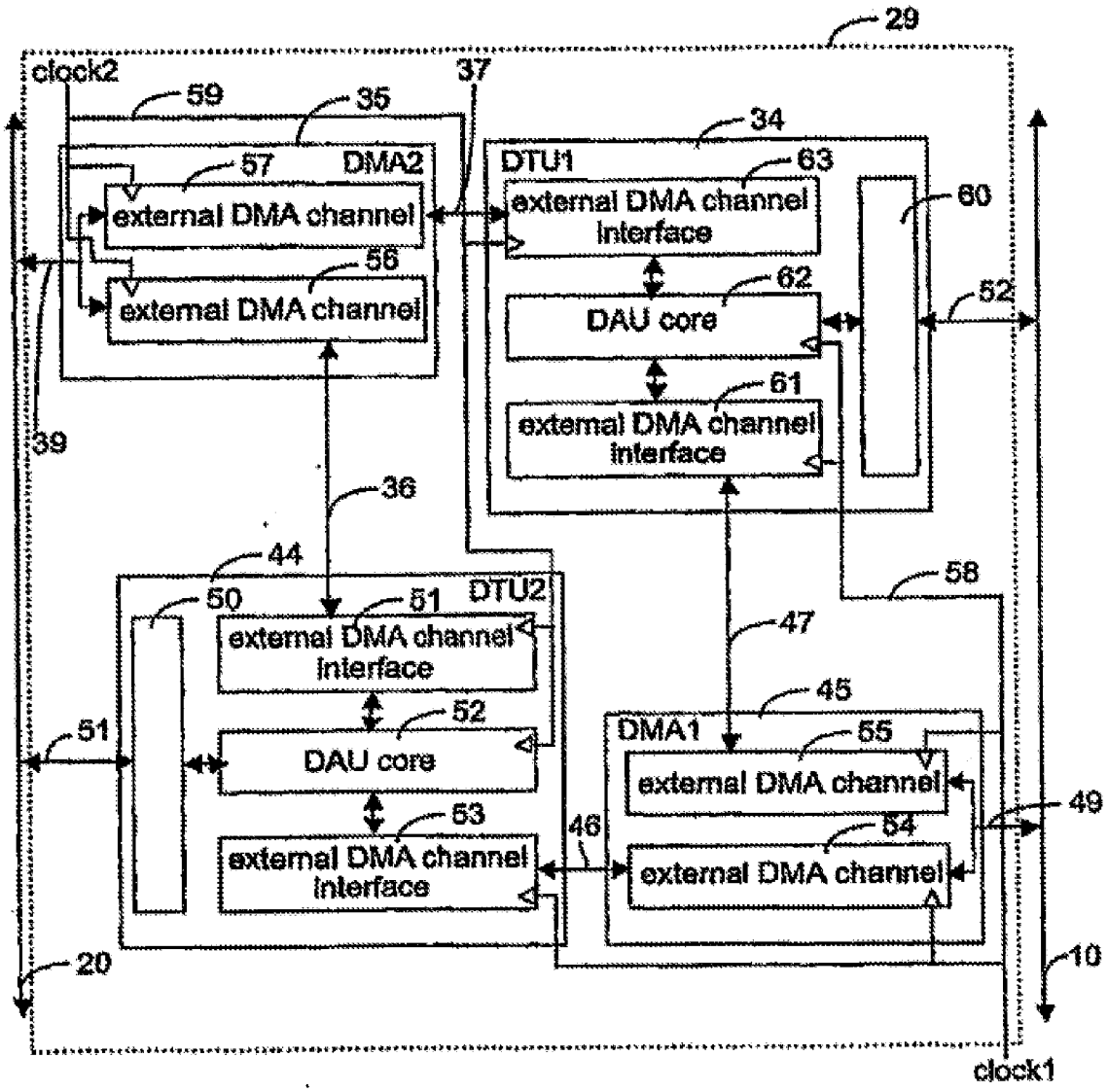

Fig. 3

Figure 3 of the Present Application

With reference primarily to Figure 3 and the description thereof on pages 9-11, an intercore communications system 29 comprises a first DTU 34 (DTU1), a second DTU 44 (DTU2), a first DMA 45 (DMA1), and a second DMA 35 (DMA2). The DMA unit 35 has two external DMA channel units 56, 57. The internal channel 39 of these two external DMA channel units 56, 57 is connected to the bus processor 20.

The first external DMA channel unit 56 is connected via a link 36 to the second DTU 44. The second external DMA channel unit 57 is connected via a link 37 to the first DTU 34. The first DMA unit 45 comprises two external DMA channel units 54, 55. The internal channel of these two external DMA channel units 54, 55 is connected to the processor bus 10. The first external DMA channel unit 55 is connected via a link 47 to the first DTU 34. The second external DMA channel unit 54 is connected via a link 46 to the second DTU 44. The internal channel 49 of these two external DMA channel units 54, 55 is connected to the bus processor 10.

The DTU 34 comprises a first processor interface 60 allowing a programming link 52 to be established via the processor bus 10 to the processor P1 (See Figure 2). The DTU 34 further comprises a direct access unit core (DAU core) 62, and two external DMA channel interfaces 61 and 63. The external DMA channel interface 61 serves as an interface to the external DMA channel unit 55 and the external DMA channel interface 63 serves as an interface to the external DMA channel unit 57.

The DTU 44 comprises a first processor interface 50 allowing a programming link 51 to be established via the processor bus 20 to the processor P2 (See Figure 2). The DTU 44 further comprises a direct access unit core (DAU core) 52, and two external DMA channel interfaces 51 and 53. The external DMA channel interface 51 serves as an interface to the external DMA channel unit 56 and the external DMA channel interface 53 serves as an interface to the external DMA channel unit 54.

The clock signal of the first processor P1 (clock 1) is fed via a clock line 58 to the following units: external DMA channel unit 54, external DMA channel unit 55, external DMA channel interface 53, external DMA channel interface 61, and DAU core 62. The clock signal of the second processor P2 (clock 2) is fed via a clock line 59 to the following units: external DMA channel unit 56, external DMA channel unit 57, external DMA channel interface 51, external DMA channel interface 63, and DAU core 52.

The processor P1 configures the first DTU 34 via the first processor interface 60. The processor P2 configures the second DTU 44 via the second processor interface 50. In both cases the external channels of the first DMA unit 45 use the resources of the internal DMA

channel 49 on the processor bus 10, and the external channels of the second DMA unit 35 use the resources of the internal DMA channel 39 on the processor bus 20.

As illustrated in Figure 3, the communication system 29 provides for clock decoupling. All of the blocks are either clocked by the clock1 of the processor P1 or by the clock2 of the processor P2 such that activity on one processor does not require simultaneous and equivalent activity on the other processor.

The Examiner initially bears the burden of establishing a *prima facie* case of unpatentability. *In re Bell*, 26 U.S.P.Q.2d 1529 (Fed. Cir. 1993); *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984); MPEP § 2142.

A rejection based on alleged anticipation may be attacked by showing that a single element is missing from the cited reference. Under 35 U.S.C. § 102, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Here, the Examiner has failed to establish a *prima facie* case of anticipation for claims 13, 14, 16, 18 and 19. The Examiner erred in asserting that Koch teaches or enables each of the claimed elements, either expressly or inherently, as interpreted by one of ordinary skill in the art.

An obviousness rejection may be attacked by showing that the Examiner has failed to properly establish a *prima facie* case or by presenting evidence tending to support a conclusion of non-obviousness. In order to find *prima facie* obviousness when combining references, MPEP § 2143(A)(1) states the following (emphasis ours): "Office personnel must articulate the following: (1) a finding that the prior art included each element claimed, although not necessarily in a single prior art reference, with the only difference between the claimed invention and the prior art being the lack of actual combination of the elements in a single prior art reference." MPEP § 706.02(j) further states (emphasis ours): "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of

reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)." *See also In re Thrift and Hemphill*, 298 F.3d 1357, 1366 (Fed. Cir. 2002) (for an examiner to establish a *prima facie* case that an invention, as defined by a claim at issue, is obvious the examiner must: (1) show some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or the combined references) must teach or suggest all the claim limitations); MPEP § 2142. Moreover, a reference must be viewed as a whole, including portions that would lead away from the claimed invention. MPEP § 2141.02 (citing *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983). If the proposed modification would change the principles of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP § 2143.01 (citing *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959)).

A. Claims 13, 14, 16, 18 and 19 Are Not Anticipated by Koch

As noted above, the Examiner entered an amendment to claim 13 for purposes of appeal, and Appellants believe the Examiner no longer contends claims 13, 14, 16, 18 and 19 are anticipated by Koch. Nevertheless, to avoid any possible waiver Appellants will address whether claims 13, 14, 16, 18 and 19 are anticipated by Koch.

Independent claim 13 recites a "system comprising: …

a first bi-directional channel to couple the second processor to the first shareable unit [comprising:]

a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and

a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and

a second bi-directional channel to couple the first processor to the second shareable unit [comprising:]

a second external channel of the first DMA unit to operate on the first processor clock; and

a second external channel of the second DMA unit to operate on the second processor clock."

In the Final Office Action, the Examiner points to Figure 4 of Koch, which shows two bi-directional channels: (i) a first channel comprising access unit 51, DMA 41, and interface 42; and (ii) a second channel comprising access unit 48, DMA 54, and interface 55. Examiner points to DMA 41 with its external interface 42 and to DMA 54 with its external interface 55. The Examiner does not identify a second external interface of the first DMA 41 or a second external interface of the second DMA 54. Further, there is no suggestion in Koch of any bidirectional channel coupling a processor to a sharable unit through an external channel from both of the DMAs 41 and 54. Accordingly, the Examiner has not established a *prima facie* case of anticipation of claim 13 by Koch at least because the Examiner has not shown that Koch discloses two bi-directional channels having a first DMA unit configured with two external channels operating on a first processor clock and a second DMA unit configured with two external channels operating on a second processor clock. Claims 16, 18 and 19 depend from claim 13 and are not anticipated by Koch at least by virtue of their dependencies.

1. Claim 14 Is Not Anticipated by Koch for Additional Reasons

Claims 14 depends from claim 13, and is not anticipated by Koch for at least the reasons set forth above with regard to claim 13. In addition, claim 14 recites "wherein the first bi-directional channel comprises: a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock." As discussed above, Koch does not teach a first bidirectional channel comprising an external channel of a first DMA and an external channel of a second DMA as recited in claim 13. Thus, Koch, alone or in combination with Tang, also does not teach, suggest or motivate a first bidirectional channel comprising a first programmable unit coupled between the first external channel of a first DMA unit and the first external channel of the second

DMA unit. In addition, the Examiner points to access unit 51, external interface 42 and DMA1 41. The Examiner does not point to a second DMA unit or an external channel of a second DMA unit. Assuming arguendo the Examiner would rely on DMA2 54, there is no indication in Koch of a bidirectional channel comprising a programming unit coupled between DMA1 41 and DMA2 54. Thus, claim 14 is not anticipated by Koch for the additional reason that Koch does not teach "a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit," as recited.

B. *Claims 1-7, 9 and 10 Are Not Rendered Obvious by Koch in View of Tang*

Independent claim 1 recites a "system comprising: …

a first processor on a first clock coupled to the first processor bus; …

a first programmable unit …

a second processor on a second clock coupled to the second processor bus; …

a second programmable unit …

wherein the first programmable unit and the second programmable unit each comprises:

a direct access unit core;

a first external direct memory access channel interface on the first clock; and

a second external direct memory access channel interface on the second clock,

wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit."

The Examiner points to access unit 51, DMA 41, interface 42, paragraphs 45, 48, 51 and 56 and Figure 4 of Koch as teaching programming elements for a first programmable unit and to access unit 48, DMA 54, interface 55 and paragraphs 45, 48, 51 and 56 as teaching programming elements for a second programmable interface. The cited portions of Koch do not disclose two programmable units each of which has two external direct memory access channel

interfaces, each on one of two clocks. The Examiner points to column 2, lines 42-55 of Tang as teaching dual external DMA channels. For convenience, Figure 4 of Koch and the cited portion of Tang are repeated below.

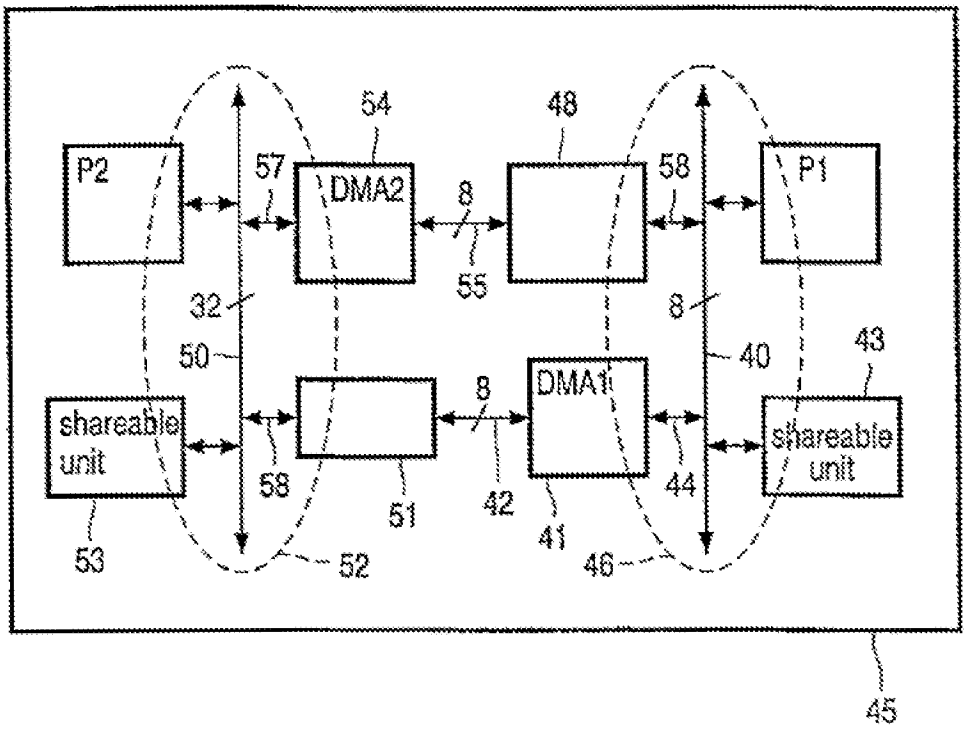

FIG. 4

Figure 4 of Koch

The cited portion of Tang recites as follows:

Yet another aspect is an apparatus for reducing latency due to set up time between DMA transfers, comprising: a first DMA channel interface participating in a current DMA transfer; a second DMA channel interface providing a DMA channel request for a next DMA transfer before the current DMA transfer is completed; and a DMA controller initiating arbitration of DMA channel requests after the DMA channel request for the next DMA transfer is provided by the second DMA channel interface and before the current DMA transfer is completed, and initiating set up for the next DMA transfer prior to completion of the current

DMA transfer according to the arbitration so as to reduce latency due to set up time between the current DMA transfer and the next DMA transfer.

Tang. Col. 2:42-55.

Tang is directed to an arbitration system for a system with a common bus clock. Tang teaches arbitration and reduction in latency between completion of a first data transfer of a first DMA channel interface and the set up of a second data transfer of a second DMA channel interface on the same bus and the same clock. See Figure 9 of Tang and the description thereof at Col. 7:31 to 8:4. There is no suggestion in Tang that the DMA channel interfaces are on separate clocks that also clock separate respective processors coupled to separate buses. Thus, the Examiner has failed to establish a *prima facie* case that each of the elements claimed is taught by the combination of Koch and Tang. To the extent the Examiner contends it would have been obvious to further modify the combination of Koch and Tang, the Examiner has not presented a convincing line of reasoning as to why the skilled artisan would have found the claimed invention to have been obvious in light of the teachings of Koch and Tang.

The motivation to which the Examiner points for making the additional modification to the combination of Koch and Tang is reducing the latency time between DMA transfers. This would seem to motivate, if anything, adding a second channel interface on a same clock, rather than motivating a second channel interface on a different clock. Accordingly, it is respectfully submitted that claims 1-7, 9 and 10 are not rendered obvious by Koch, alone or in combination with Tang, because the combination of Koch with Tang does not teach, disclose or motivate "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock," as recited.

C. Claims 13-19 Are Not Rendered Obvious by Koch, Alone or in Combination with Tang

Independent claim 13 recites, a "system comprising:

a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock;

a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock;

a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface to the second processor, wherein the first bi-directional channel comprises:

a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and

a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and

a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus, wherein the second bi-directional channel comprises:

a second external channel of the first DMA unit to operate on the first processor clock; and

a second external channel of the second DMA unit to operate on the second processor clock."

The Examiner points to Figure 4 of Koch, which shows two separate bi-directional channels: (i) a first channel of access unit 51, DMA 41, and interface 42; and (ii) a second channel of access unit 48, DMA 54, and interface 55. There is no suggestion in Koch of that either bidirectional channel comprises a external channel from both DMA1 41 and from DMA2 54. Adding a second channel to either of the DMAs of Koch, which the Examiner contends is motivated by Tang, does not teach, suggest or motivate a bidirectional channel comprising an external channel from two separate DMAs, let alone two bidirectional channels each comprising an external channel from each of two DMAs. Thus, Koch, alone or in combination with Tang, does not teach, suggest, motivate or otherwise render obvious a system

comprising: a first bi-directional channel having a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock and a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and a second bi-directional channel having a second external channel of the first DMA unit to operate on the first processor clock and a second external channel of the second DMA unit to operate on the second processor clock. Accordingly, claim 13, as well as claims 14-19 that depend from claim 13, are not rendered obvious by Koch, alone or in combination with Tang.

1. Claim 14 Is Not Rendered Obvious by Koch, Alone or in Combination with Tang for Additional Reasons

Claims 14 depends from claim 13, and is not rendered obvious by Koch for at least the reasons set forth above with regard to claim 13. In addition, claim 14 recites "wherein the first bi-directional channel comprises: a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock." As discussed above, Koch does not teach a first bidirectional channel comprising an external channel of a first DMA and an external channel of a second DMA as recited in claim 13. Thus, Koch, alone or in combination with Tang, also does not teach, suggest or motivate a first bidirectional channel comprising a first programmable unit coupled between the first external channel of a first DMA unit and the first external channel of the second DMA unit. In addition, the Examiner points to access unit 51, external interface 42 and DMA1 41. The Examiner does not point to a second DMA unit or an external channel of a second DMA unit. Assuming arguendo the Examiner would rely on DMA2 54, there is no indication in Koch of a bidirectional channel comprising a programming unit coupled between DMA1 41 and DMA2 54. Tang does not supply the missing teaching. Thus, claim 14 is not rendered obvious by Koch, alone or in combination with Tang, for the additional reason that the combination does not teach "a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit," as recited.

2. Claim 15 Is Not Rendered Obvious by Koch, Alone or in Combination with Tang for Additional Reasons

Claims 15 depends from claims 13 and 14, and is not rendered obvious by Koch, alone or in combination with Tang, for at least the reasons set forth above with regard to claims 13 and 14. In addition, claim 15 recites "a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock." As discussed above, Koch, alone or in combination with Tang, does not teach, suggest or motivate a second bidirectional channel comprising an external channel of a first DMA and an external channel of a second DMA as recited in claim 13, and it does not disclose a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock, as recited in claim 14. Thus, Koch, alone or in combination with Tang, also does not teach "a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock." Assuming, arguendo, the Examiner would rely on DMA1 41 and DMA2 54 as the recited first and second DMAs, there is no indication of any programmable unit coupled between DMA1 41 and DMA2 54, let alone of two programmable units coupled as recited. Accordingly, claim 15 is not rendered obvious by Koch, alone or in combination with Tang, for the additional reason that the combination does not teach, suggest or motivate "a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock," as recited.

D. Conclusion of Argument

The Examiner has failed to establish a *prima facie* case that the claims are anticipated or rendered obvious by Koch, whether considered alone or in combination with Tang. Accordingly, the Examiner's rejections cannot be sustained and reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,
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VIII. CLAIMS APPENDIX

1. A System comprising:

a first processor bus;

a first processor on a first clock coupled to the first processor bus;

a first direct memory access unit with a first external direct memory access channel, the first direct memory access unit being coupled to the first processor bus;

a first programmable unit comprising a first processor interface, the first programmable unit coupled via the first external direct memory access channel to the first direct memory access unit, said first programmable unit being programmable by the first processor via the first processor interface;

a first shareable unit coupled to the first processor bus;

a second processor bus;

a second processor on a second clock coupled to the second processor bus;

a second direct memory access unit with a second external direct memory access channel, the second direct memory access unit being coupled to the second processor bus;

a second programmable unit comprising a second processor interface, the second programmable unit coupled via the second external direct memory access channel to the second direct memory access unit, said second programmable unit being programmable by the second processor via the second processor interface; and

a second shareable unit being connected to the second processor bus,

wherein the first programmable unit and the second programmable unit each comprises:

a direct access unit core;

a first external direct memory access channel interface on the first clock; and

a second external direct memory access channel interface on the second clock,

wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit.

2. The system of claim 1, wherein the first bi-directional communication channel and/or the second bi-directional communication channel are half-duplex channels or full-duplex channels.

3. The system of claim 1, wherein the first processor and the second processor are similar from an architectural point of view.

4. The system of claim 1, wherein the first processor and the second processor are implementations of the same type of processor design.

5. The system of claim 1, wherein the first processor and the second processor are implementations of different types of processor design.

6. The system of claim 1, wherein the first and second shareable units each comprise one of the following: a memory, a peripheral, an interface, an input device, an output device.

7. The system of claim 1, wherein one of the first and second processors comprises a central processing unit, a microprocessor, a digital signal processor, a system controller, a co-processor, or an auxiliary processor.

9. The system of claim 1, wherein each processor interface has a programming link either for connecting to a corresponding processor bus or for connecting to a corresponding processor.

10. The system of claim 1, wherein the first and second bi-directional communication channels are configured to transfer data and/or control information to and from the first and second shareable units.

13. A system comprising:

a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock;

a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock;

a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface to the second processor, wherein the first bi-directional channel comprises:

a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and

a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and

a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus, wherein the second bi-directional channel comprises:

a second external channel of the first DMA unit to operate on the first processor clock; and

a second external channel of the second DMA unit to operate on the second processor clock.

14. The system of claim 13, wherein the first bi-directional channel comprises:

a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock.

15. The system of claim 14, wherein the second bi-directional channel comprises:

a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock.

16. The system of claim 13, wherein the first bi-directional channel comprises:

a first external channel of a common programmable unit, the first external channel operating on the second processor clock, and the first external channel also coupled to the first external channel of the second DMA unit;

a second external channel of the common programmable unit, the second external channel to operate on the first processor clock, and the second external channel also coupled to the first external channel of the first DMA unit; and

a first programmable core of the common programmable unit, the first programmable core to operate on the second processor clock, the first programmable core coupled between the first and second external channels of the common programmable unit and the first programmable core comprising the first programming interface to the second processor.

17. The system of claim 16, wherein the second bi-directional channel comprises

a third external channel of the common programmable unit, the third external channel to operate on the second processor clock, and the third external channel also coupled to the second external channel of the second DMA unit;

a fourth external channel of the common programmable unit, the fourth external channel to operate on the first processor clock, and the fourth external channel also coupled to the second external channel of the first DMA unit; and

a second programmable core of the common programmable unit, the second programmable core to operate on the first processor clock, the second programmable core coupled between the third and fourth external channels of the common programmable unit and the second programmable core comprising the second programming interface to the first processor.

18. The system of claim 13, wherein the first bi-directional channel further comprises a first master configured to initiate data transfers with active devices on the first or second busses.

19. The system of claim 13, wherein the second bi-directional channel further comprises a second master configured to initiate data transfers with active devices on the first or second busses.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.